1 Introduction

From lecture and homework, you have studied the benefits of a cache memory. In this lab you will investigate for yourself whether or not the Atmel AT91SAM7L microcontroller utilizes a cache memory and provide a summary of your findings and reasoning. You may find it necessary to recall the documentation that is provided on the lab webpage under Reference Documents. Note that an additional document has been added - the ARM Architecture Reference Manual. Source code has also been provided for you to perform experimentation with the microcontroller yourself.

2 Lab Procedure

2.1 Study the Documentation

1. Use the resources on the lab webpage to research about the AT91SAM7L and the ARM7TDMI core. Wikipedia also has a nice summary of ARM processors (http://en.wikipedia.org/wiki/ARM_Architecture).
2. Refer to the documentation directly in a summary of your research findings.

2.2 Test Your Theory

1. Download the source code from the lab webpage. Inside the lab05 workspace, you will find a program that has been setup specifically for testing the memory access time. It is a very simple program that simply fills an array with data and then reads the entire contents of the array 1000 times to amplify the subtle differences in the memory access time. It uses the serial port for communication of its results.
2. You may find it useful to refer to the Timer Counter section (section 10.10 on pages 42 and 419 of the AT91SAM7L Datasheet - AT91SAM7L128/64 Preliminary).
3. Run an experiment on the AT91SAM7L. Vary the ARRAY_SIZE variable through its complete range to thoroughly test the resulting difference in memory access times.
4. Change the ARRAY_TYPE to char and repeat the experiment with an array of chars. Note that the maximum array size is higher when testing chars.
5. Plot the average number of TC0 timer counts per inner loop vs ARRAY_SIZE for both int and char.

2.3 Analysis

1. Analyze the plot. Describe the characteristics of the curves. Point out any notable traits.
2. Document your experimental findings. How do they compare to your research findings?
3. Does the AT91SAM7L have a cache?

3 Lab Report

Your lab report should contain the following items:

1. A research summary from studying the documentation. Assert whether or not the AT91SAM7L has a cache memory from studying the documentation.
2. The plot of the average number of TC0 timer counts per inner loop vs ARRAY_SIZE for each the integer and character case.
3. An analysis of the experimental results as well as an analysis of the plot.
4. A final conclusion on the presence of the cache on the AT91SAM7L microcontroller.